DEPARTMENT OF ELECTRICAL ENGINEERING

IIT(ISM), DHANBAD-826004

SEM: 3rd (B. TECH)

COURSE NAME: ANALOG AND DIGITAL ELECTRONICS LAB

COURSE CODE: EEC272

LOCATION: ROOM No. 115

List of Experiments:

DEPARTMENT OF ELECTRICAL ENGINEERING

IIT(ISM), DHANBAD-826004

SEM: 3rd (B. TECH)

COURSE NAME: ANALOG AND DIGITAL ELECTRONICS LAB

COURSE CODE: EEC272

LOCATION: ROOM No. 115

EXPT. NO. 1

TITLE: Study of Astable Multivibrator using 555 timer

DO'S and DON'TS:

1. Make sure that connections are made with proper pins.
2. Restrict the voltage to 5V only, avoid fluctuations.
3. Check for polarity of capacitor, leds for proper connections working.
4. The resistance and capacitor should be chosen appropriately so that T_{ON} and T_{OFF} can be measured accurately.

AIM: To design and study of Astable Multivibrator using 555 timer and determine duty ratio.

THEORY:

When IC555, a combination of linear comparator and digital flip-flops is to be configured as an astable multivibrator, both the trigger and threshold inputs (pin2, 6) to the two comparators are connected together and to a capacitor. The capacitor charges towards the supply voltage through 2 resistors R_1 and R_2.The discharge pin7 connected to the internal transistor is connected to the junctions of those two resistors. When Power is first applied to the circuit, the capacitor will unchanged therefore both trigger and the threshold inputs will be near zero volts. This also turns of transistor T_1.

This allows the capacitor to begin charging through R_1 and R_2.As soon as the charge on the capacitor reaches 2/3 of the supply voltage, the upper comparator will trigger causing the flip-flop to reset. Which causes the output to switch low. The effect of T_1 conducting causes resistor $R_2$to be connected across the external capacitor .Resistor R_2 is effected connected to ground through internal transistor T_1. The result of output is a continuous stream of rectangular pulses**.**

CIRCUIT DIAGRAM:

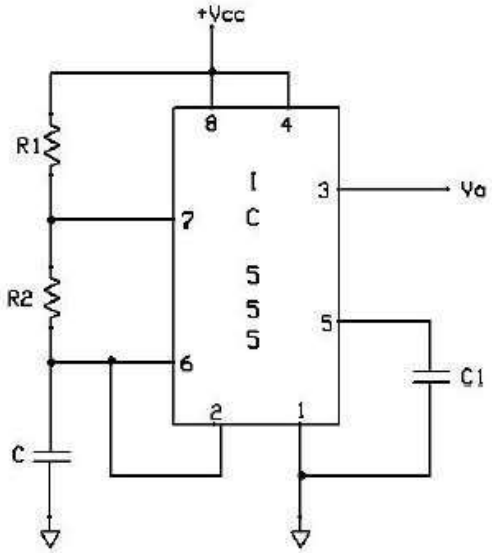

Figure 1 : Pin Diagram of 555 timer IC (Values: R_1=470KΩ, R_2=470KΩ, C=2.2microF, C_1=0.01microF)

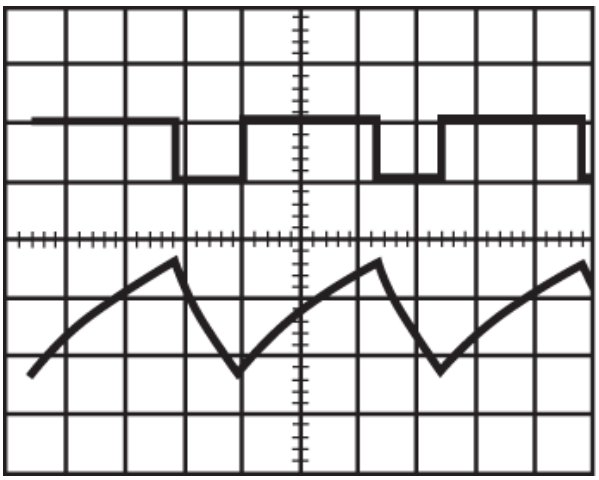

Figure 2 :Output Voltage and Capacitor Voltage

APPARATUS REQUIRED:

Sl. No.	Instruments/Apparatus	Maker's Name	Specification	Quantity
1	IC 555			
2	Resistors			
3	Capacitors			
4	Project Board			
5	DC Power Supply			

PROCEDURE:

- Connections are made as per the circuit diagram.
- Observe *the output waveform of Schmitt trigger circuit by giving sine wave* as input**.**
- Note down the amplitude and time period and draw the output waveform.

OBSERVATION TABLE:

Experimental		**Calculated**		**%Error**	
T_{ON}(sec)	**T_{OFF}(sec)**	**T_{ON}(sec)**	**T_{OFF}(sec)**	**T_{ON}**	**T_{OFF}**

RESULTS:

The error from the above experimental values for T_{on} that is_____% and that for T_{off} is _____%. This shows that formula used for theoretical calculations work satisfactory.

SAMPLE QUESTIONS:

1. What is free running frequency of Astable multivibrator?
2. Astable multivibrator operating at 150Hz has a discharge time of 2.5m. Find the duty cycle of the circuit.
3. How to obtain symmetrical waveform in Astable multivibrator?

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EXPT. NO. 2

TITLE: Verification of precision half wave rectifier and full wave rectifier using OP-AMP.

DO'S and DON'TS:

1. Observe all ratings and mark on the instruments to avoid fire and shocks.
2. Do not operate in wet/damp condition.
3. Do not operate in explosive atmosphere.
4. Keep the product dust free, clean and dry.

AIM: To verify the output voltage of precision half wave rectifier and full wave rectifier using OP-AMP

THEORY:

The major limitation of ordinary diodes is that it cannot rectify voltage below 0.6V, the cut-in voltage of the diode. The precision rectifier, which is also known as a super diode, is a configuration obtained with an operational amplifier in order to have a circuit behaving like an ideal diode and rectifier. It can be useful for high-precision signal processing.

Half Wave Rectifier:

A half wave rectifier is an electronic circuit. The rectifier circuit takes alternating current. from the wall outlet and converts it into a positive direct current (DC) output. The particular electronic device that accomplishes this task is a semiconductor called a diode. The diode like all semiconductors is a material which has a resistance in between that of a condor wire and an insulator like that of a plastic.

Full Wave Rectifier:

A Full rectifier is a circuit which converts an ac voltage into a pulsating dc voltage using both half cycles of the applied ac voltage. It uses two diodes of which one conduct during one half cycle while the other conducts during the other half cycle of the applied ac voltage.

During the positive half cycle of input voltage, diode D1 becomes forward biased and D2 becomes reverse biased. Hence D1 conducts and D2 remains OFF. The load current flows through D1 and the voltage drop across R_L will be equal to the input voltage. During the negative biased. Hence D1 remains OFF and D2 conduct. The load current flows through D2 and the voltage drop across R_L will be equal to the input voltage.

CIRCUIT DIAGRAM:

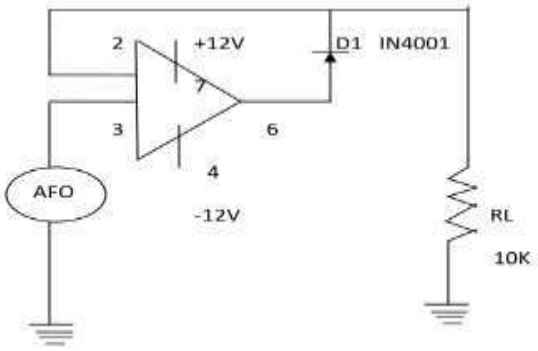

Figure 1. Precision half wave rectifier

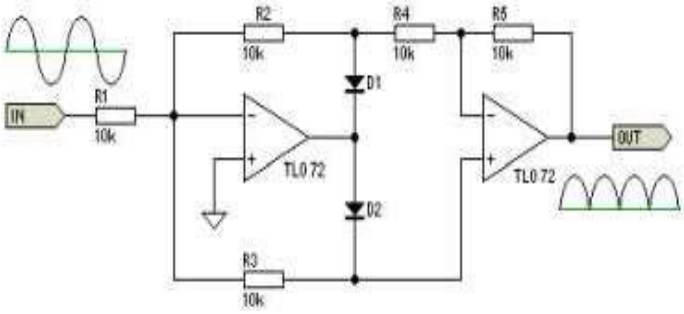

Figure 2. Full wave precision rectifier

Model Graphs:

Figure 3. Model graph for half wave precision rectifier

Figure 4. Model graph for full wave precision rectifier

APPARATUS REQUIRED:

SI. No.	Apparatus	Range	Quantity
1	Trainer Kit		
2	CRO		
3	Multi meter		
4	Connecting wires		

PROCEDURE:

1. Connections are made as shown in circuit diagram.

2. A sinusoidal input of frequency 100Hz and amplitude 0.5V is applied from a function generator.

3. Rectified output is observed on the CRO. To get equal amplification in both cycles the DC offset from function generator is carefully adjusted.

4. Input and output voltage levels are noted.

5. A plot of Vo V/S Vi plotted by feeding Vi to channel A and Vo to channel B and time knob to X via A mode.

OBSERVATION:

- For half wave rectifier

SI. No.	Input voltage	Output Voltage	% error

- For full wave rectifier

SI. No.	Input voltage	Output Voltage	% error

RESULT:

Thus the half wave rectifier and full wave rectifier are constructed and the output waveforms are drawn.

SAMPLE QUESTIONS:

1. Draw the circuit of a full wave rectifier and explain how it gives the average value?
2. What is a Clipper and Clamper Circuit?
3. Draw the circuit of a clipper which will clip the input signal below a reference voltage.
4. Draw the equivalent circuit of a full wave rectifier for input voltage less than zero volts (Vi<0).

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LOCATION: ROOM No. 115

EXPT. NO. 3

TITLE: Study of op-amp as an Inverting and Non Inverting Summer

DO'S and DON'TS:

1. All the connections should be made properly.
2. IC should not be reversed.
3. Keep the product dust free, clean and dry.

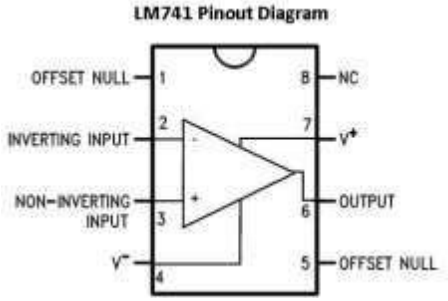
AIM: To study the Summing operation of Op-amp in inverting and non inverting configuration.

THEORY:

An operational amplifier or op-amp is a linear integrated circuit that has a very high voltage gain, high input impedance and low output impedance. Op-amp is basically a differential amplifier whose basic function is to amplify the difference between two input signals.

Op-amp has five basic terminals, that is, two input terminals, one o/p terminal and two power supply terminals. Pin2 is called the inverting input terminal and it gives opposite polarity at the output if a signal is applied to it. It produces a phase shift of 180º between input and output. Pin3 is called the non-inverting terminal that amplifies the input signal without inversion, i.e., there is no phase shift or i/p is in phase with o/p. The op-amp usually amplifies the difference between the voltages applied to its two input terminals. Two further terminals pins 7 and 4 are provided for the connection of positive and negative power supply voltages respectively. Terminals 1 and 5 are used for dc offset. The pin 8 marked NC indicates 'No Connection'.

Figure 1. Op-Amp Pin Diagram



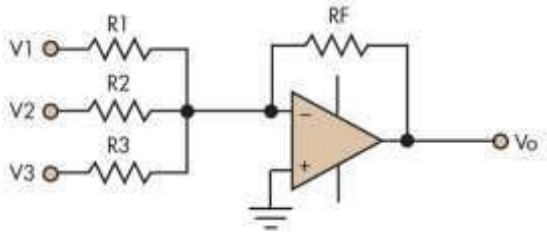


Figure 2 (a). Op amp as Inverting Summer

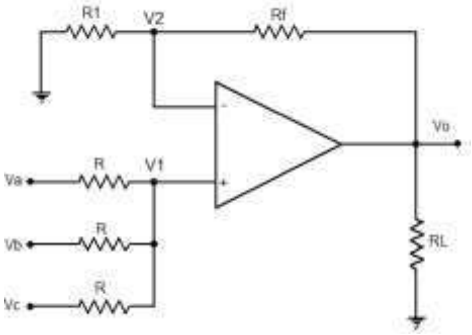


Figure 2 (b). Op amp as Non Inverting Summer

APPARATUS REQUIRED:

Sl. No.	Instruments/Apparatus	Range	Quantity
1	Experiment Board, ST2322	-	-
2	Multimeter	-	-
3	Patch cords	-	-

PROCEDURE:

(A) Inverting Summer:

1. Set the value of Resistance R1, R2, R3 and Rf as 10KΩ.
2. Connect the on board firs variable power supply to input socket 'IN10', and then set the input voltage $V_1$to 0.5 V.
3. Connect the on board firs variable power supply to input socket 'IN11', and then set the input voltage V_2 to 0.5 V.
4. Insert the Multi-meter's positive probe at TP12's Sockets and negative probe at the ground.
5. Calculate the output voltage V_{OUT} by using equation 1.
6. Note the Measured output V_{OUT}'.
7. Verify the measured output voltage to Calculated Output Voltage.
8. Vary the input Voltages $V_1$and V_2.
9. Repeat the above step from 4 to 7 for every variation in input.

(B) Non Inverting Summer:

1. Connect the on board firs variable power supply to input socket 'IN12', and then set the input voltage V_1 to 0.5 V.
2. Connect the on board firs variable power supply to input socket 'IN13', and then set the input voltage $V_1$to 0.5 V.
3. Insert the Multi-meter's positive probe at TP14's Sockets and negative probe at the ground.
4. Set the Value of Resistances R as 10KΩ, R1 and Rf at 1KΩ.
5. Calculate the output voltage V_{OUT} by using equation 2.
6. Note the Measured output V_{OUT}'.
7. Verify the measured output voltage to Calculated Output Voltage.
8. Vary the input Voltages $V_1$and V_2.
9. Repeat the above step from 4 to 7 for every variation in input.

OBSERVATIONTABLE:

(a) Inverting Summer:

S. No.	Input voltage V_1	Input Voltage V_2	Output Voltage(Calculated) V_{OUT}	Output Voltage(Measured) V_{OUT}'	Error= I_{OUT}- I_{OUT}'

(b) Non Inverting Summer:

S. No.	Input voltage V_1	Input Voltage V_2	Output Voltage(Calculated) V_{OUT}	Output Voltage(Measured) V_{OUT}'	Error= V_{OUT}- V_{OUT}'

CACULATION:

For inverting summer $$V_0 = -R_f\left(\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3}\right) \quad (1)$$

For Non Inverting Summer $$V_0 = \left(\frac{V_a + V_b + V_c}{3}\right)\left(1 + \frac{R_f}{R_1}\right) \quad (2)$$

RESULTS:

Op-amp as an inverting and non-inverting amplifier has been studied and verified.

SAMPLE QUESTIONS:

1. The following circuit represents an inverting scaling amplifier. Compute the value of R_{om} and V_O?

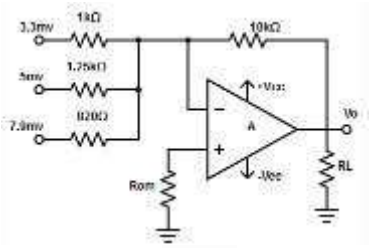


Fig. 3

2. Determine the expression of output voltage for inverting summing amplifier consisting of four internal resistors? (Assume the value of internal resistors to be equal)
3. Determine the expression of output voltage for non-inverting summing amplifier consisting of four internal resistors? (Assume the value of internal resistors to be equal)

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COURSE NAME: ANALOG AND DIGITAL ELECTRONICS LAB

COURSE CODE: EEC272

LOCATION: ROOM No. 115

EXPT. NO. 4

TITLE: Study of op-amp as a differential amplifier

DO'S and DON'TS:

1) Use only main cord designed for the instrument.
2) Observe all ratings and marks on the instrument to avoid fire and shock hazards.
3) Do not operate in wet/damp conditions.
4) Do not operate in explosive atmosphere.
5) Keep the product dust free, clean and dry.

AIM: To study op-amp as a differential amplifier and observing its output at noisy signal common to both input terminal.

THEORY:

The *differential amplifiers* amplify the difference between two voltages making this type of operational amplifier circuit a Subtractor unlike a summing amplifier which adds or sums together the input voltages. This type of operational amplifier circuit is commonly known as a Differential Amplifier configuration. By connecting each input in turn to 0V ground we can use superposition to solve for the output voltage V_{OUT}. Then the transfer function for a Differential Amplifier circuit is given as:

$$V_{OUT} = -V_1\left(\frac{R_3}{R^1}\right) + V_2\left(\frac{R_4}{R^2 + R^4}\right)\left(\frac{R_1 + R_3}{R^1}\right)$$

When resistors, $R_1 = R_2$ and $R_3 = R_4$ the above transfer function for the differential amplifier can be simplified to the following expression:

$$V_{OUT} = \frac{R_3}{R_1}(V_2 - V_1)$$

If all the resistors are all of the same ohmic value, that is: $R_1 = R_2 = R_3 = R_4$ then the circuit will become a **Unity Gain Differential Amplifier** and the voltage gain of the amplifier will be exactly one or unity. Then the output expression would simply be $V_{OUT} = V_2 - V_1$. Also note

that if input V_1 is higher than input V_2 the output voltage sum will be negative, and if V_2 is higher than V_1, the output voltage sum will be positive.

The Differential Amplifier circuit is a very useful op-amp circuit and by adding more resistors in parallel with the input resistors R_1 and R_3, the resultant circuit can be made to either "Add" or "Subtract" the voltages applied to their respective inputs. One of the most common ways of doing this is to connect a "Resistive Bridge" commonly called a *Wheatstone Bridge.*

Circuit Diagram of Op-amp as a differential amplifier is shown below :-

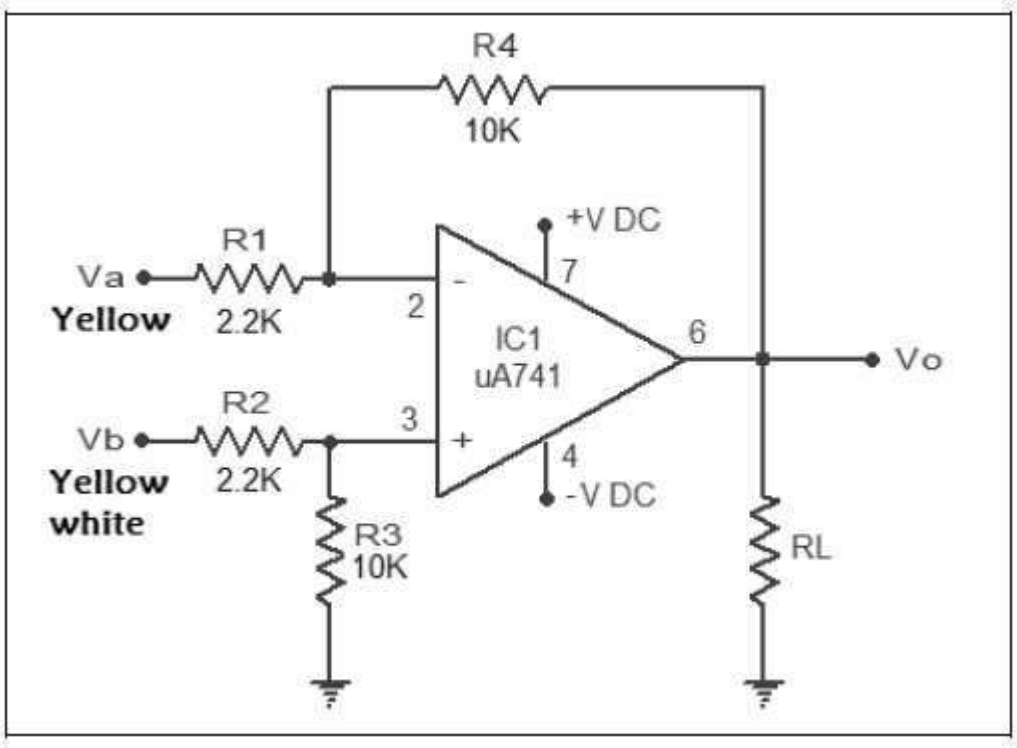

Figure 1. Differential Amplifier.

APPARATUS REQUIRED:

SI. No.	Instruments/Apparatus	Range	Quantity
1	Experiment board, ST2322		
2	Oscilloscope		
3	2 mm patch cords		
4	Multi-meter		

PROCEDEURE:

1) Connect the relevant circuit for the difference configuration as shown in the circuit diagram.
2) Measure the output voltage V_{OUT} from Kit.
3) Observe the waveforms at V_1, V_2, and V_{OUT}.
4) Note the phase of the output voltage $V_0$with respect to the input voltage.
5) Set different values of two input voltages, and find the output voltage
6) Repeat the steps 3, 4, and 5.
7) The waveforms are to be plotted.

OBSERVATION:

SI. No.	Input voltage (+ve) V_1	Input Voltage (-ve) V_2	Output voltage V_{OUT} (measured)	Output Voltage $V_{OUT'}$ (measured)	Error=V_{OUT}-$V_{OUT'}$

RESULTS:

The measured and calculated differential voltage is the same.

SAMPLE QUESTIONS:

1) Define CMRR.
2) Give the use of current mirror circuit in differential amplifier.
3) Draw the basic circuit of differential amplifier using BJT. Give the significance of R_C and R_{EE}.

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SEM: 3rd (B. TECH)

COURSE NAME: ANALOG ELECTRONICS LABORATORY

COURSE CODE: EEC13212

LOCATION: ROOM No. 115

EXPT. NO. 5

TITLE: Study of Class B Amplifier operation

DO'S and DON'TS:

1) Use only main cord designed for the instrument.
2) Observe all ratings and marks on the instrument to avoid fire and shock hazards.
3) Do not operate in wet/damp conditions.
4) Do not operate in explosive atmosphere.
5) Keep the product dust free, clean and dry.

AIM: To study the operation of Class B amplifier and determine crossover distortion span (per cycle) at different loading condition.

THEORY:

The class A amplifiers are the amplifiers which deliver maximum undistorted symmetrical output voltage swing to the low impedance load. Generally, any system (like a stereo, radio or television) consists of several stages of amplification. When the signal passes through these stages, the power level of signal rises so much that the later stages require high power handling circuit elements such as power transistors. Also, as the load impedance of these later stages is very small (of the order of 8 ohm for stereo amplifier speakers), heavy collector current flows. To handle this, transistors having power rating of 1W or more are used in power amplifiers.

Power amplifiers are broadly classified as:

1. Class A (VoltageAmplifier)
2. Class B (Push-Pull EmitterFollower)
3. Class C TunedAmplifier

Class B Amplifier:

Class B amplifier is a circuit in which transistor conducts (collector current flows) for only 180° of input AC signal. When a signal is applied, one half cycle will forward bias the base-emitter junction and Ic will flow. The other half cycle will reverse bias the base-emitter junction and Ic will be cut off.

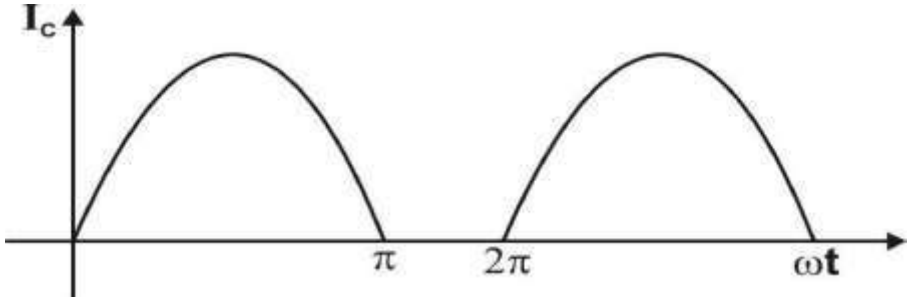
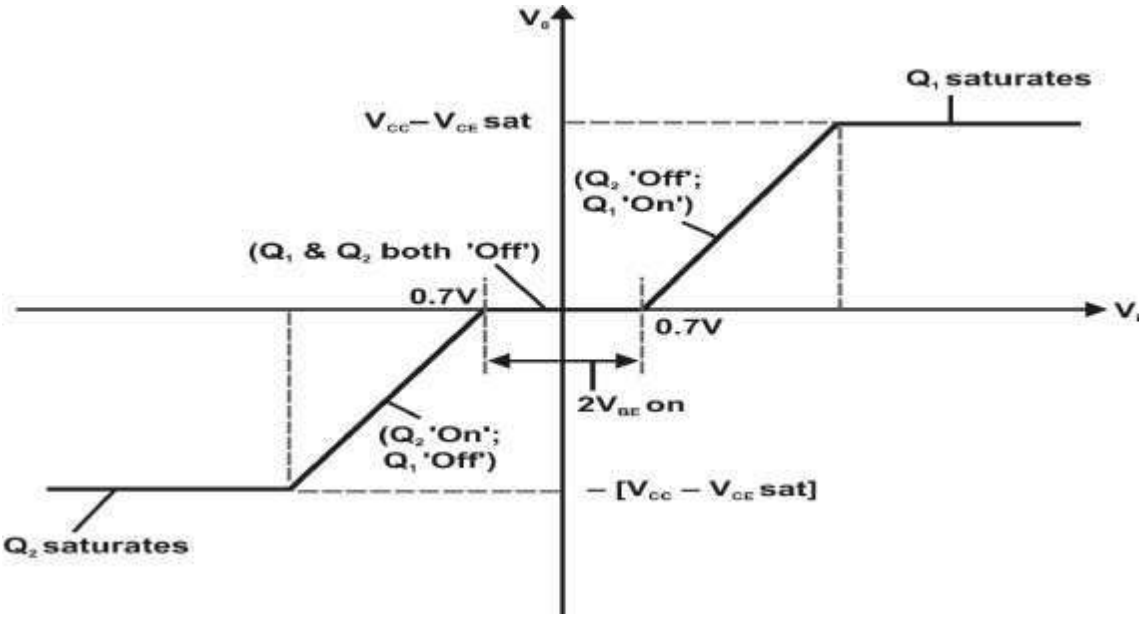


Figure 1. Collector current waveform.

For class B amplifiers the Q point is located near the cutoff point of the load line. Thus, to amplify entire input AC signal a combination of two Class - B amplifiers are used. One of which amplifies positive half cycle of input AC signal and the other amplifies negative half cycle of input AC signal. This amplifier configuration is known as push-pull or complementary symmetry. In the push-pull configuration it is important to match the two transistors carefully for the proper amplification of both the halves. While the input signal being amplified through class B amplifier the input signal has to rise to about 0.7V to overcome the barrier potential of amplifying transistor. During this period no current flows through the circuit and output is zero. The action is similar for both the transistors. Thus, following characteristic is obtained for input and output voltages:

Figure 2. Input-output characteristic.



The output signal no longer remains sine wave and gets distorted. Since the clipping occurs between the time when one transistor cuts off and at the time when other one comes on. We call it **crossover distortion.**

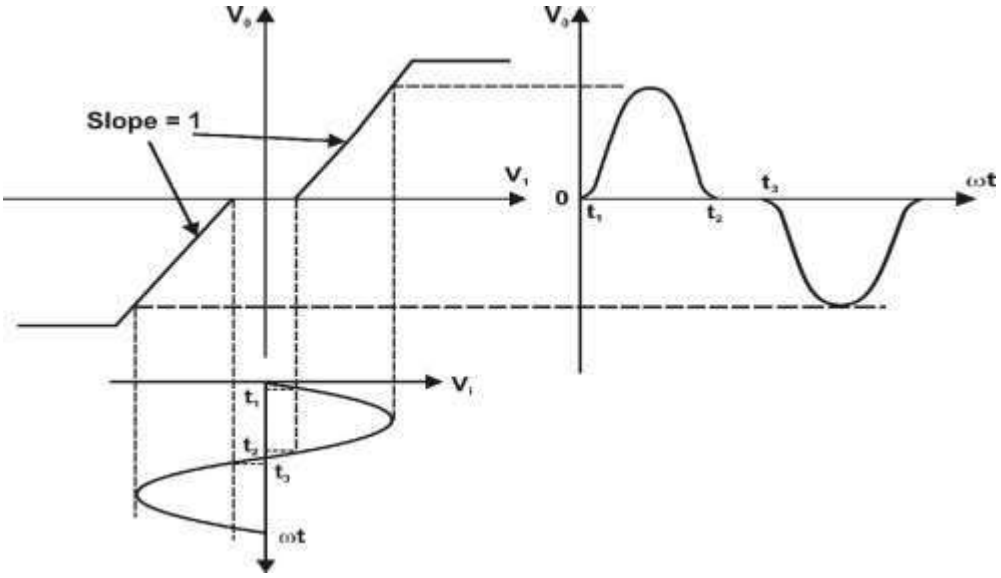


Figure 3. Input and output waveforms illustrating the zone/crossover distortion.

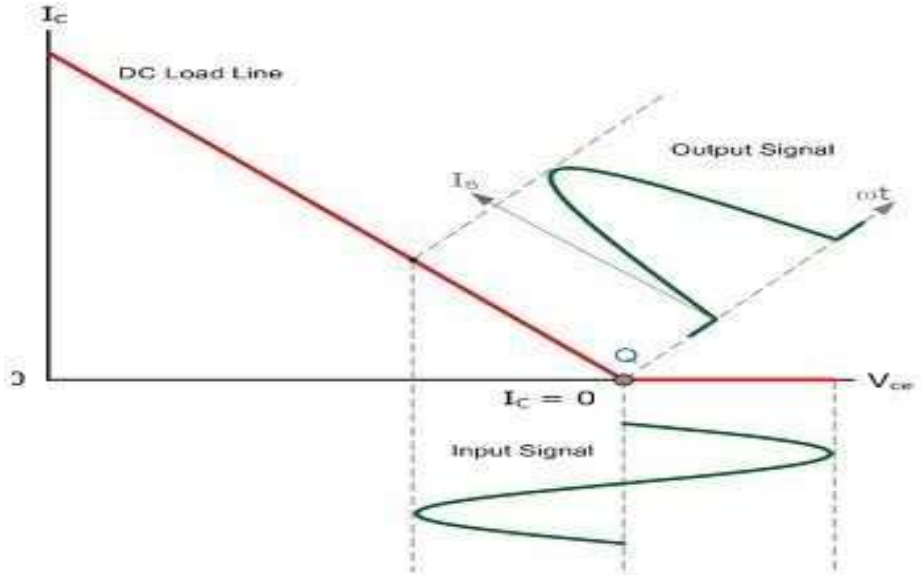


Figure 4. Output Characteristics Curves for class B amplifier

Class B Amplifiers have the advantage over their Class A amplifier in that no current flows through the transistors when they are in their quiescent state (i.e. with no input signal), therefore no power is dissipated in the output transistors or transformer when there is no signal present unlike Class A amplifier stages that require significant base bias thereby dissipating lots of heat - even with no input signal. So, the overall conversion efficiency (η) of the amplifier is greater than that of the equivalent Class A with efficiencies reaching as high as 75% possible resulting in nearly all modern types of push-pull amplifiers operated in this Class B mode.

Complementary-Symmetry Class B Push-Pull Amplifier:

Class B push-pull amplifier also called as Complementary-Symmetry Class B Amplifier circuit it is shown below. While Class B amplifiers have a much high gain than the Class

A types, one of the main disadvantages of class B type push-pull amplifiers is that they Suffer from an effect known commonly as Crossover Distortion. This occurs during the transition when the transistors are switching over from one to the other as each transistordoes not stop or start conducting exactly at the zero crossover point even if they are specially matched pairs. This is because the output transistors require a base-emitter voltage greater than 0.7V for the bipolar transistor to start conducting which results in both transistors being "OFF" at the same time. This then would give us what is commonlycalled a Class AB Amplifier circuit.

The circuit diagram of Class B Amplifier :-

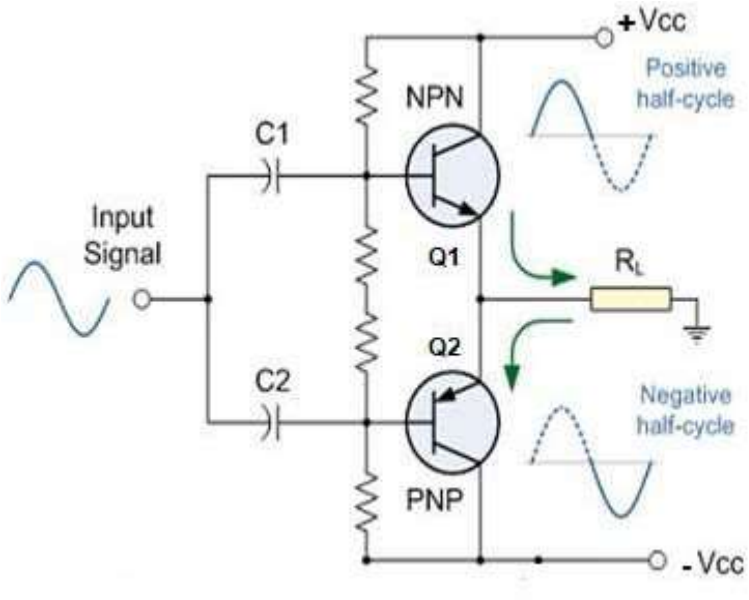


Figure 5. Class B amplifier

APPARATUS REQUIRED:

SI. No.	Instruments/Apparatus	Range	Quantity
1	Power amplifier trainer kit NV6522		
2	2 mm patch cords		
3	Oscilloscope		

PROCEDURE:

1. Connect **+5V** and **-5V** DC power supplies at their indicated position from DC Voltage Supply to Class 'B' Power Amplifier & also '**Gnd**' toground.

2. Now connect the "**Output**" of Frequency Generator to "**Vin**." of Class 'B' Power Amplifier and as well as connectground.

3. Connect CRO channel 1 to sockets '**Vin**' and '**Gnd**' of Class 'B' Power Amplifier using the CRO probe.

4. Put the VR3 to its minimum position i.e. rotate it fully anticlockwise. (This is the condition when no bias voltage is applied to the emitter diodes of both thetransistors.)

5. Now switch On thesupply.

6. Using the '**Frequency Control'** and '**Amplitude Control'** knobs of the Function Generator, set the input signal at 2VppVoltage, 10 KHz frequency and observe it on

.

7. Connect Oscilloscope (channel 2) at the '**Vout'** and '**Gnd'** terminals of Class 'B' Power Amplifier and observe the output waveform. The crossover distortion can be clearly observed on the oscilloscope.

Note: For observing I/P & O/P waveform simultaneously keep the Oscilloscope at **Dual** mode.

8. Gradually increase the bias voltage by increasing bias resistance VR3 (i.e. rotate the VR3in clockwise direction) up to the value when the crossover distortion is completely removed and maximum amplification of the input signal isobtained.

9. Now observe the amplitude of input & output signal and calculate the voltage gain. (The class B amplifier has unity voltagegain)

Observations:

Sl. No	**Frequency**	**Crossover distortion span (per cycle) in degree**	**peak magnitude**	
			Input voltage	**Output voltage**

SAMPLE QUESTIONS:

1) Discuss crossover distortion in class B power amplifier.
2) Prove that the theoretical conversion efficiency of class B amplifier.
3) What is the power dissipation capability of each transistor used, in terms of maximum power output of the amplifier?
4) What are the advantages of class B amplifier?

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SEM: 3rd (B. TECH)

COURSE NAME: ANALOG AND DIGITAL ELECTRONICS LAB

COURSE CODE: EEC272
LOCATION: ROOM No. 115

EXPT. NO. 6

TITLE: Study of Class A amplifier operation

DO'S and DON'TS:

1) Use only main cord designed for the instrument.
2) Observe all ratings and marks on the instrument to avoid fire and shock hazards.
3) Do not operate in wet/damp conditions.
4) Do not operate in explosive atmosphere.
5) Keep the product dust free, clean and dry.

AIM: To study the operation of Class A amplifier and determine voltage gain.

THEORY:

The class A amplifiers are the amplifiers which deliver maximum undistorted symmetrical output voltage swing to the low impedance load. Generally, any system (like a stereo, radio or television) consists of several stages of amplification. When the signal passes through these stages, the power level of signal rises so much that the later stages require high power handling circuit elements such as power transistors. Also, as the load impedance of these later stages is very small (of the order of 8 ohm for stereo amplifier speakers), heavy collector current flows. To handle this, transistors having power rating of 1W or more are used in power amplifiers.

Power amplifiers are broadly classified as:

1. Class A (Voltage Amplifier)
2. Class B (Push-Pull Emitter Follower)
3. Class C Tuned Amplifier

Class A Amplifier:

Class A amplifier is basically a voltage amplifier in which transistor operates in active region for the entire cycle of input AC signal. In other words the collector current flows for 360° of AC signal.

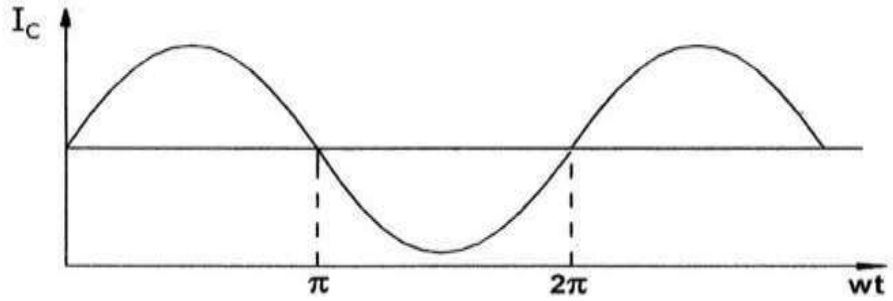

Figure 1. Collector current waveform.

For class A amplifiers the Q point is located somewhere near the middle of the AC load line and thus offers maximum amplification of the input signal as shown below:

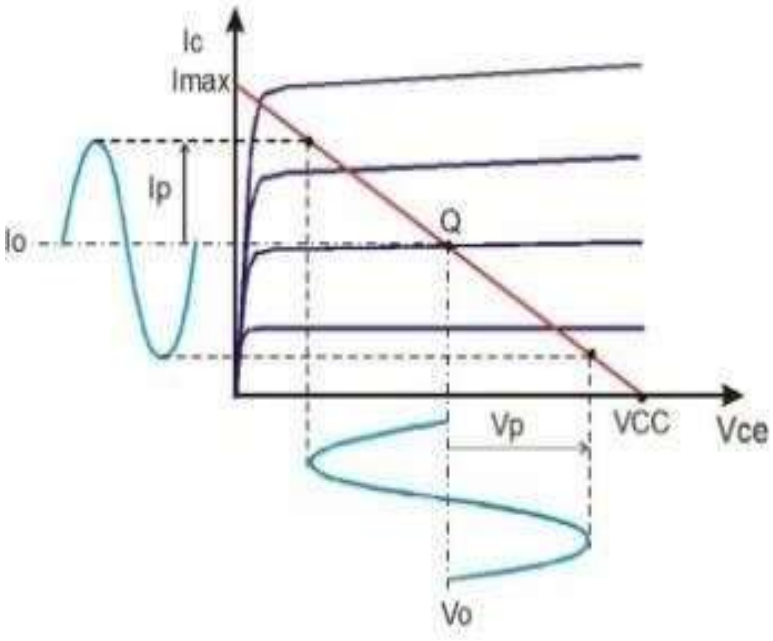

Figure 2. Output characteristic

The collector current IC is non-zero even when the input signal is zero i.e. the IC flows for 100% of time. This leads to power dissipation even in quiescent condition. The Class ‘A’ amplifier is the most common and simplest form of power amplifier that uses the switching transistor in the standard common emitter circuit configuration. The transistor is always biased "ON" so that it conducts during one complete cycle of the input signal waveform producing minimum distortion and maximum amplitude to the output. This means that the Class ‘A’ Amplifier configuration operates in the ideal operating mode, because there can be no crossover or switch-off distortion to the output waveform even during the negative half of the cycle. Class ‘A’ power amplifier output stages may use a single power transistor or pair of transistors connected together to share the high load current.

This is the simplest type of Class A power amplifier circuit. It uses a single-ended transistor for its output stage with the resistive load connected directly to the collector terminal. When the transistor switches "ON" it sinks the output current through the collector resulting in an inevitable voltage drop across the emitter resistance thereby limiting the negative output capability. The efficiency of this type

of circuit is very low (less than 30%) and delivers small power outputs for a large drain on the DC power supply. Class 'A' amplifier stage passes the load current even when no input signal is applied. So, large heat sinks are needed for the output transistors.

The Class A amplifier uses the same transistor for both halves of the output waveform and due to its biasing arrangement, the output transistor always has current flowing through it, even if there is no input signal. In other words, the output transistor never turns "OFF". This results in very low efficiency as its conversion of the DC supply power to the AC signal power delivered to the load is usually very low. Generally, the output transistor of a Class A amplifier gets very hot even when there is no input signal present. So some form of heat sinking is required. The DC current flowing through the output transistor (Ic) when there is no output signal will be equal to the current flowing through the load.

The circuit diagram of Class A amplifier is shown below:

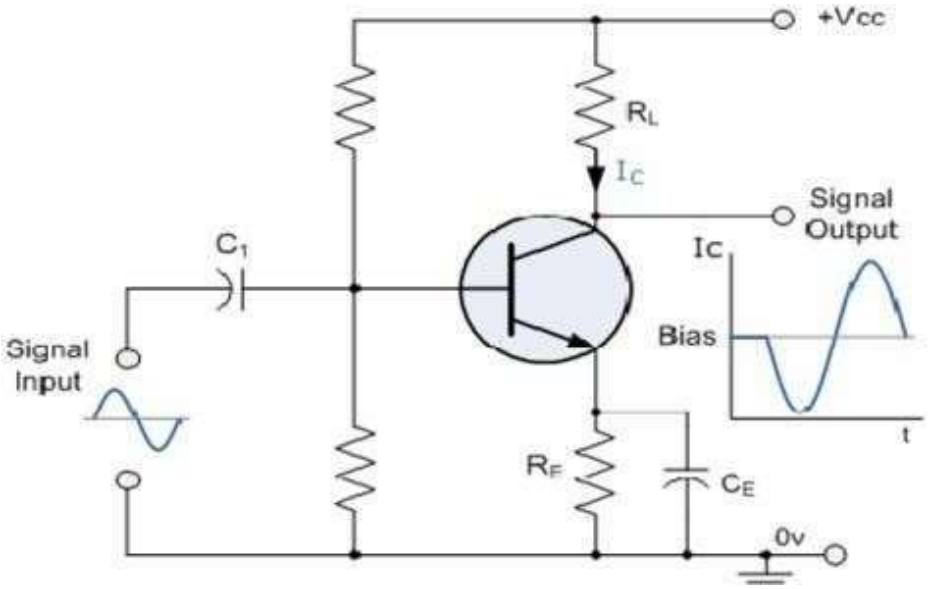

Figure 3. Class A amplifier

APPARATUS REQUIRED:

SI. No.	Instruments/Apparatus	Range	Quantity
1	Power amplifier trainer kit NV6522.		
2	2 mm patch cords		
3	Oscilloscope		

PROCEDURE:

1. Connect the +12V DC supply to '+12V' of Class 'A' Amplifier and also 'Gnd' to ground as shown in circuit diagram.
2. Now connect the "Output" of Frequency Generator to "Vin." of Class 'A' Power Amplifier and as well as connect ground.
3. Connect CRO channel 1 to sockets 'Vin' & 'Gnd' of Class 'A' Power Amplifier using the CRO probe.
4. Set the VR1 and VR2 fully anticlockwise direction.
5. Now switch On the supply.
6. Using the 'Frequency Control' and 'Amplitude Control' knobs of the Function

Generator, set the input signal at 2Vp-pVoltage, 10 KHz frequency and observe it on Oscilloscope (channel1).

Note: Keep peak to peak voltage of input signal less than 4Vpp to avoid saturation of amplifier.

7. Connect CRO channel 2 to sockets 'Vout' &'Gnd' of Class 'A' Power Amplifier using CRO probe.
8. Vary VR2 gradually towards clockwise direction up to the maximum amplification of the output signal is obtained.
9. Observe the amplified output on Oscilloscope (channel 2) with positive clipping.
10. Now vary VR1 in clockwise direction, you will observe the +ve clipping disappears which shows that the Q-point is shifting downwards along the DC load line.
11. Observe the amplified output on Oscilloscope (channel 2) which is 4Vpp approximately and also observe the phase shift of180°.

OBSERVATION:

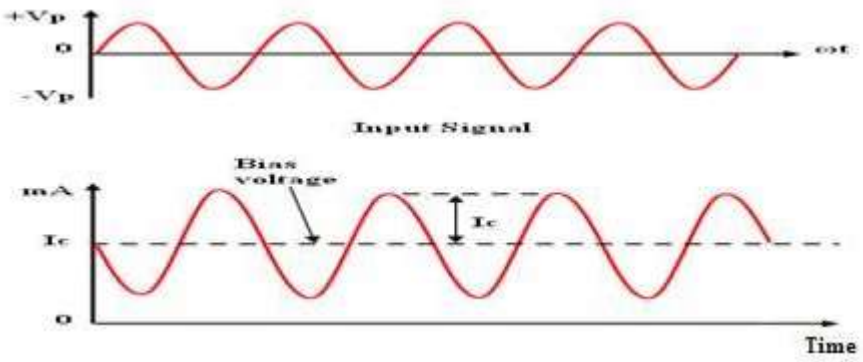

Fig. 4. Class A Output Waveform

RESULTS:

Input ac signal amplitude (Vin)..... Vp-p
Output ac signal amplitude (Vout) .....Vp-p
Voltage Gain (**Av**) = **Vout**/**Vin**.....

SAMPLE QUESTIONS:

1. What is a power amplifier? In what respect it is different from Voltage amplifier?
2. Why heat sink is required?
3. What are the disadvantages of class A amplifier?

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SEM: 3rd (B. TECH)

COURSE NAME: ANALOG AND DIGITAL ELECTRONICS LAB

COURSE CODE: EEC272
LOCATION: ROOM No. 115

EXPT. NO. 7

TITLE:-Study of logic gates.

APPARATUS REQUIRED:-

SL.NO.	Instruments/Apparatus	Specification	Quantity
1.	AND GATE	IC 7408	1
2.	0R GATE	IC 7432	1
3.	NOT GATE	IC 7404	1
4.	NAND GATE 2 I/P	IC7400	1
5.	NOR GATE	IC7402	1
6.	X-OR GATE	IC7486	1
7.	Power supply	230V,50HZ	1
8.	LED	-	1
9.	Bread board	-	1
10.	Patch cord	-	-

THEORY:
Circuit that takes the logical decision and the process are called logic gats, Each gates has one and more input and only one output.
OR, AND and NOT are basic gates .NAND, NOR and X-OR are known as universal logic gates. Basic gates from these gates.

PROCEDURE:

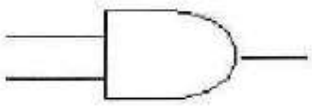
(1) Connections are given as per circuit diagram.
(2) Logical inputs are given as per circuit diagram.
(3) Observe the output and verify the truth table.

CIRCUIT DIAGRAM:

(1) AND Gate

Y=A.B

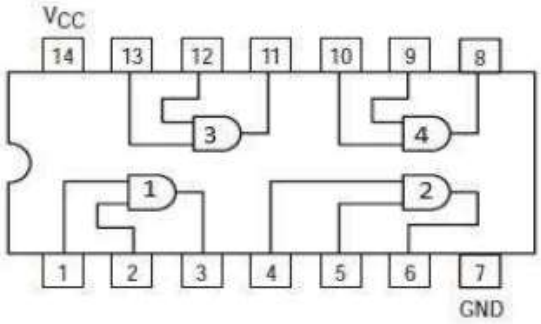
SYMBOL:-



TRUTH TABLE:-

A	B	Y=A.B
0	0	0
0	1	0
1	0	0
1	1	1

Pin Diagram:-



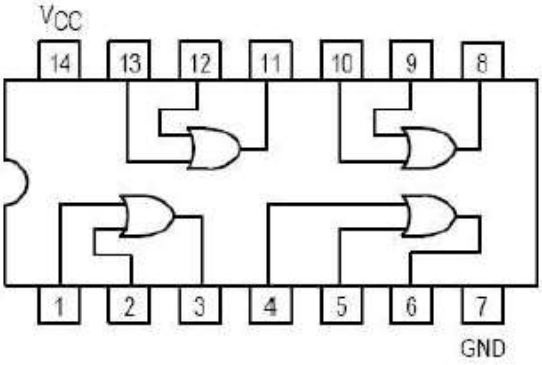
(2) OR Gate
Y=A+B

SYMBOL:

TRUTH TABLE:

		A+B

PIN DIAGRAM:-



(3) **NOT GATE**

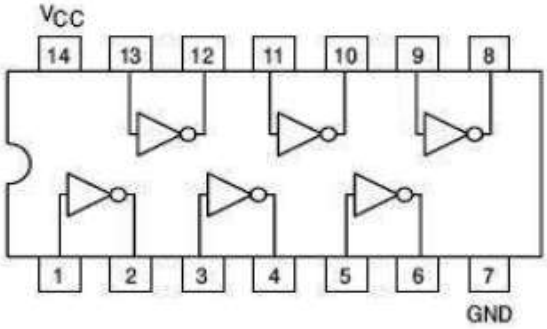
Y= $\bar{A}$

Symbol:

TRUTH TABLE:-

A	**Y=** $\bar{A}$
0	**1**
1	**0**

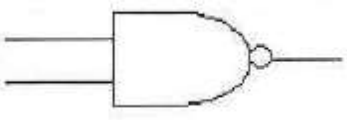
PIN DIAGRAM:-



(4.) NAND GATE:-

Y= $\overline{A.B}$

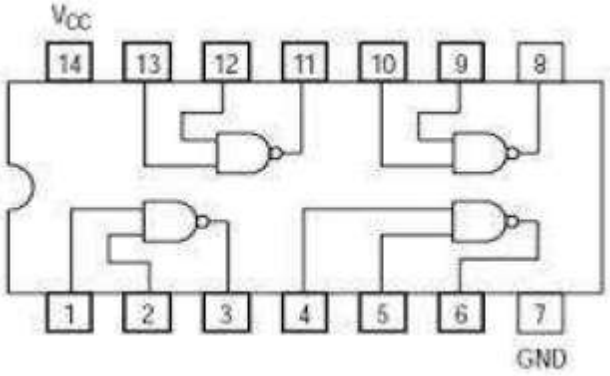
SYMBOL:-



TRUTH TABLE:-

A	**B**	**Y=** $\overline{A.B}$
0	0	1
0	1	1
1	0	1
1	1	0

PIN DIARAM:-



(5.)NOR GATE:

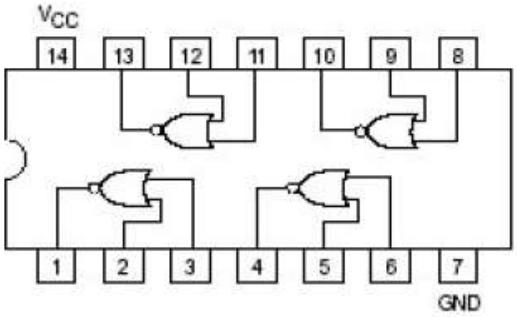
$Y = \overline{A + B}$

SYMBOL:- **TRUTH**

TABLE:-

A	B	Y=$\overline{A + B}$
0	0	1
0	1	1
1	0	1
1	1	0

PIN DIARAM:-

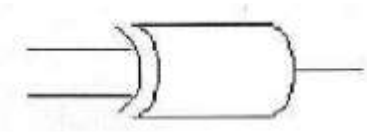


(6.) X-OR GATE:-

Y=$A\overline{B}+B\overline{A}$

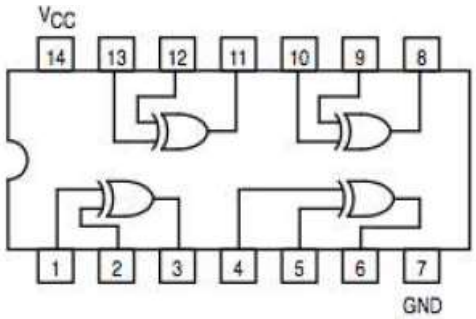
SYMBOL:- **TRUTH**

TABLE:-



A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

PIN DIAGRAM:-



RESULTS:-

The Truth table of logic gates were verified.

PRECAUTIONS:-

1. Connection should be tight.
2. Wear Shoes while working with electrical equipment.
3. Power supply should be given after checking the circuit.

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COURSE CODE: EEC272
LOCATION: ROOM No. 115

EXPT. NO. 8

TITLE:- To realize half and full adder using IC 7400 NAND Gate.

APPARATUS REQUIRED:-

SI. No.	Instruments/Apparatus	Range	Quantity
1	Bread board		
2	74LS00 IC		
3	2 mm patch cords		
4	LED		
5	Power Supply		

THEORY:

Half-Adder:

A combinational logic circuit that performs the addition of two data bits, A and B, is called a half-adder. Addition will result in two output bits; one of which is the sum bit, S, and the other is the carry bit, C. The Boolean functions describing the half-adder are:

$$\text{Sum} = A \oplus B \qquad \text{Carry} = A\,B$$

Therefore, sum produces 1 when A&B are different and carry is 1when A&B are 1. Application of Half adder is limited.

Full-Adder:

The half-adder does not take the carry bit from its previous stage into account. This carry bit from its previous stage is called carry-in bit. A combinational logic circuit that adds two data bits, A and B, and a carry-in bit, Cin , is called a full-adder. The Boolean functions describing the full-adder are:

$$\text{Sum} = (x \oplus y) \oplus \text{Cin} \qquad \text{Carry} = xy + \text{Cin}\,(x \oplus y)$$

Therefore, sum produces one when I/P is containing odd no's of one & carry is one when there are two or more one in I/P.

CIRCUIT DIAGRAM:-

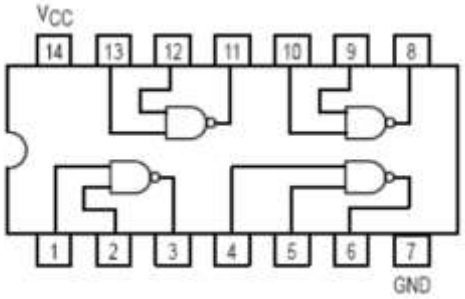

Figure1: Pin Diagram IC 7400

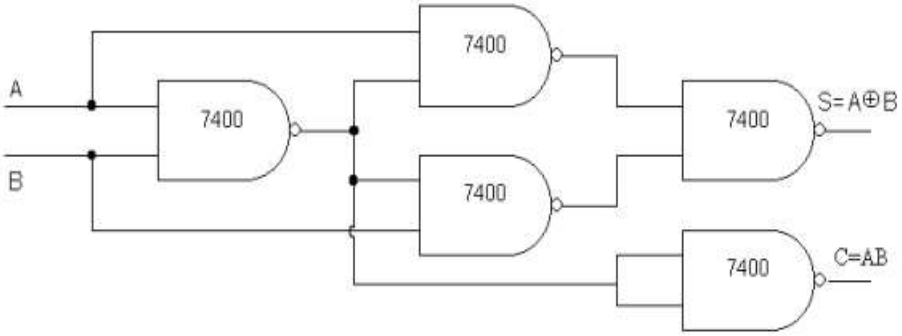

Figure2: Half Adder using NAND Gate

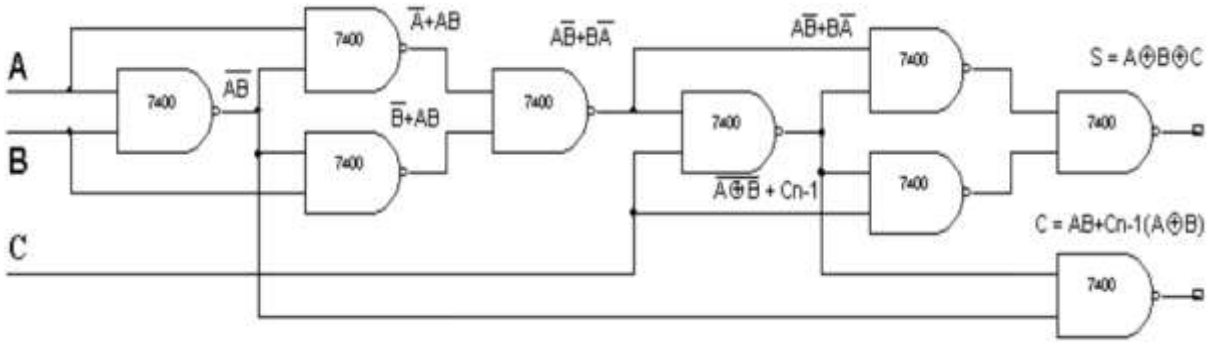

Figure3: Full Adder using NAND Gate

PROCEDEURE:-

1. Insert the IC's into the bread board.
2. Identify the i/p and o/p pin using the pin diagram.
3. Connect the bread board to a power supply of 5Vand ground the ICs.
4. Connect logic sources to the inputs of the adder.
5. Connect output from SUM and CARRY to logic indicators (LEDs).
6. Apply various input combinations to the adder.
7. Observe the SUM and CARRY outputs, verify the truth table for each input/ output combination.
8. Switch off the ac power supply.

OBSERVATION:-

Truth Table of Half Adder

A	B	Sum	Carry
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Truth Table of Full Adder

A	B	C	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

RESULTS:-

Truth table for half and full adder verified using IC 7400 NAND Gates.

PRECAUTIONS:-

1) Use only main cord designed for the instrument.
2) Observe all ratings and marks on the instrument to avoid fire and shock hazards.
3) Do not operate in wet/damp conditions.
4) Do not operate in explosive atmosphere.
5) Keep the product dust free, clean and dry.

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LOCATION: ROOM No. 115

EXPT. NO. 9

TITLE:- To realize half and full subtractor using IC 7400 NAND Gate.

APPARATUS REQUIRED:-

SI. No.	Instruments/Apparatus	Range	Quantity
1	Bread board		
2	74LS00 IC		
3	2 mm patch cords		
4	LED		
5	Power Supply		

THEORY:

Half Subtractor: Subtracting a single-bit binary value B from another A (i.e. A -B) produces a difference bit D and a borrow out bit B-out. This operation is called half subtraction and the circuit to realize it is called a half subtractor. The Boolean functions describing the half Subtractor are:

$$D = A \oplus B \qquad \text{Borrow} = A' B$$

Full Subtractor: Subtracting two single-bit binary values, B, C from a single-bit value A produces a difference bit D and a borrow out Br bit. This is called full subtraction. The Boolean functions describing the full-subtractor are:

$$D = (A \oplus B) \oplus C \qquad \text{Borrow} = A'B + A' (C) + B (C)$$

Therefore, sum produces one when I/P is containing odd no's of one & carry is one when there are two or more one in I/P.

CIRCUIT DIAGRAM:-

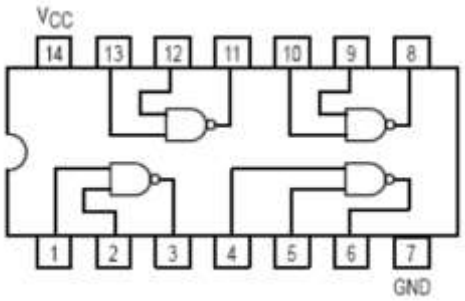

Figure1: Pin Diagram IC 7400

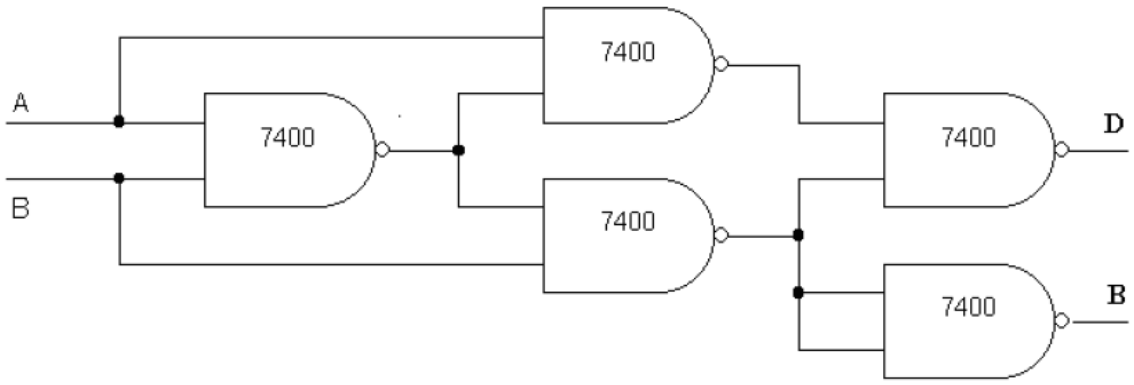

Figure2: Half Subtractor using NAND Gate

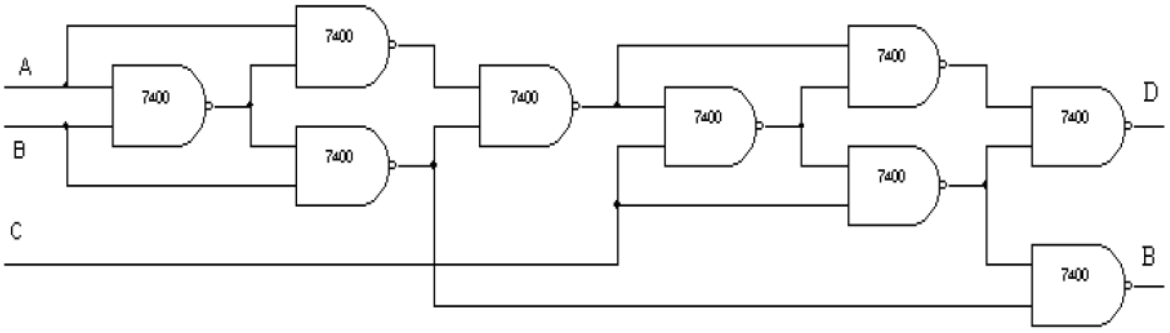

Figure3: Full Subtractor using NAND Gate

PROCEDEURE:-

1. Insert the IC's into the bread board.
2. Identify the i/p and o/p pin using the pin diagram.
3. Connect the bread board to a power supply of 5V and ground the ICs.
4. Connect logic sources to the inputs of the Subtractor.
5. Connect output from Difference and Borrow to logic indicators (LEDs).
6. Apply various input combinations to the Subtractor.
7. Observe the Difference and Borrow outputs, verify the truth table for each input/ output combination.
8. Switch off the ac power supply.

OBSERVATION:-

Truth Table of Half Subtractor

A	**B**	**D**	**Borrow**
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

Truth Table of Full Subtractor

A	B	C_{n-1}	D	Borrow
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

RESULTS:-

Truth table for half and full Subtractor verified using IC 7400 NAND Gates.

PRECAUTIONS:-

6) Use only main cord designed for the instrument.
7) Observe all ratings and marks on the instrument to avoid fire and shock hazards.
8) Do not operate in wet/damp conditions.
9) Do not operate in explosive atmosphere.
10) Keep the product dust free, clean and dry.

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SEM: 3rd (B. TECH)

COURSE NAME: ANALOG AND DIGITAL ELECTRONICS LAB

COURSE CODE: EEC272
LOCATION: ROOM No. 115

EXPT. NO. 10

TITLE: - Study of D and J-K flip flop..

APPARATUS REQUIRED:-

SI. No.	Apparatus	Range	Quantity
1	Digital IC trainer kit		
2	CRO		
3	Connecting wires		

THEORY:-
A Flip Flop is a sequential device that samples its input signals and changes its output states only at times determined by clocking signal. Flip Flops may vary in the number of inputs they possess and the manner in which the inputs affect the binary states.

D FLIP FLOP:
To eliminate the undesirable condition of indeterminate state in the SR Flip Flop when both inputs are high at the same time, in the D Flip Flop the inputs are never made equal at the same time. This is obtained by making the two inputs complement of each other.

JK FLIP FLOP:
The indeterminate state in the SR Flip-Flop is defined in the JK Flip Flop. JK inputs behave like S and R inputs to set and reset the Flip Flop. The output Q is ANDed with K input and the clock pulse, similarly the output Q' is ANDed with J input and the Clock pulse. When the clock pulse is zero both the AND gates are disabled and the Q and Q' output retain their previous values. When the clock pulse is high, the J and K inputs reach the NOR gates. When both the inputs are high the output toggles continuously. This is called Race around condition and this must be avoided.

LOGIC SYMBOL:-

(a) FOR D FLIP FLOP

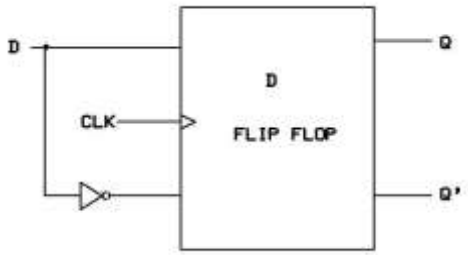

Figure1: Logic symbol of D flip flop

CHARACTERISTIC TABLE:-

CLOCK PULSE	INPUT D	PRESENT STATE (Q)	NEXT STATE(Q+1)	STATUS
1	0	0	0	
2	0	1	0	
3	1	0	1	
4	1	1	1	

Table 1: Characteristic Table of D flip flop

(b) FOR J-K FLIP FLOP

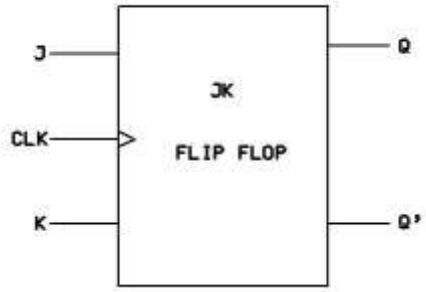

Figure2: Logic symbol of J-K flip flop

CLOCK PULSE	INPUT		PRESENT STATE (Q)	NEXT STATE(Q+1)	STATUS
	J	K			
1	0	0	0	0	
2	0	0	1	1	
3	0	1	0	0	
4	0	1	1	0	
5	1	0	0	1	
6	1	0	1	1	
7	1	1	0	1	
8	1	1	1	0	

Table 2: Characteristic Table of J-K flip flop

RESULT:

The Characteristic tables of RS, D, JK, T flip flops were verified.

PRECASUTIONS:-

1. Observe all ratings and mark on the instruments to avoid fire and shocks.
2. Do not operate in wet/damp condition.
3. Do not operate in explosive atmosphere.
4. Keep the product dust free, clean and dry.

SAMPLE QUESTIONS:-

1. What is the difference between Flip-Flop & latch?
2. Give examples for synchronous & asynchronous inputs?
3. What are the applications of different Flip-Flops?
4. What is the advantage of Edge triggering over level triggering?
5. What is the relation between propagation delay & clock frequency of flip-flop?
6. What is race around in flip-flop & how to overcome it?
8. List the functions of asynchronous inputs?

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COURSE NAME: ANALOG AND DIGITAL ELECTRONICS LAB

COURSE CODE: EEC272
LOCATION: ROOM No. 115

EXPT. NO. 11

TITLE:- Design of 3-bit Synchronous Counters

APPARATUS REQUIRED:-

S. No	Instruments/Apparatus	specification	Quantity
1	Digital Trainer Kit(DTKP-1)	-	-
2	Patch cords	-	-

THEORY:-
Circuits for counting events are frequently used in computers and other digital systems. Since a counter circuit must remember its past states, it has to possess memory. The number of flip flops used and how they are connected determine the number of states and the sequence of the states that the counter goes through in each complete cycle. Counters can be classified into two broad categories according to the way they are clocked:

A. Asynchronous (Ripple) Counters - the first flip-flop is clocked by the external clock pulse, and then each successive flip -flop is clocked by the Q or Q' output of the previous flip -flop.

B. Synchronous Counters - all memory elements are simultaneously triggered by the same clock.

SYNCHRONOUS COUNTERS:-
In synchronous counters, the clock inputs of all the flip-flops are connected together and are triggered by the input pulses. Thus, all the flip-flops change state simultaneously (in parallel). The circuit below is a 3-bit synchronous counter. The J and K inputs of FF0 are connected to HIGH. FF1 has its J and K inputs connected to the output of FF0, and the J and K inputs of FF2 are connected to the output of an AND gate that is fed by the outputs of FF0 and FF1. After the 3rd clock pulse both outputs of FF0 and FF1 are HIGH. The positive edge of the 4th clock pulse will cause FF2 to change its state due to the AND gate.
The most important advantage of synchronous counters is that there is no cumulative time delay because all flip -flops are triggered in parallel. Thus, the maximum operating frequency for this counter will be significantly higher than for the corresponding ripple counter.

CIRCUIT DIAGRAM:-

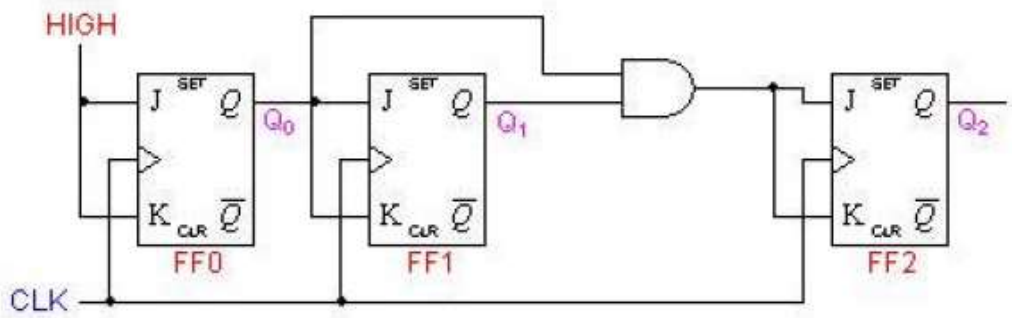

Figure 1:- Logic Diagram of 3-bit synchronous counter

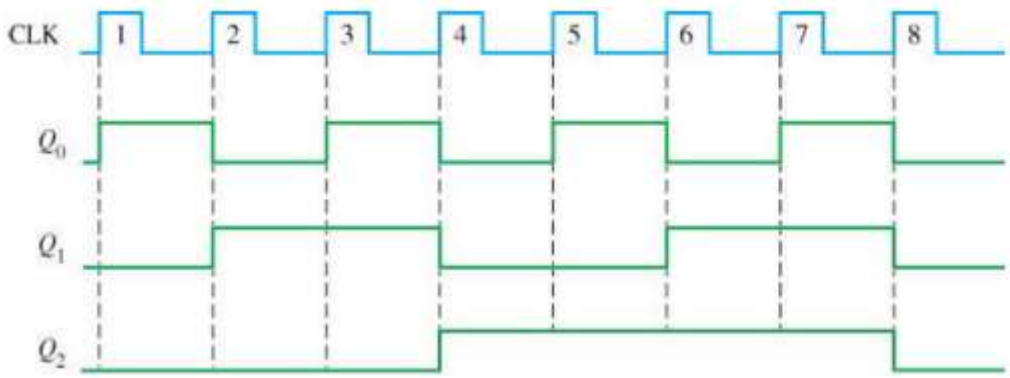

Figure 2:- Timing Diagram of 3-bit Counter

PROCEDURE:-

1. Construct the logic circuit as shown in figure 1.
2. Use the up/(down)' input to choose up counter or down counter.
3. Verify the count sequence as given in figure 4.

LOGIC DIAGRAM:-

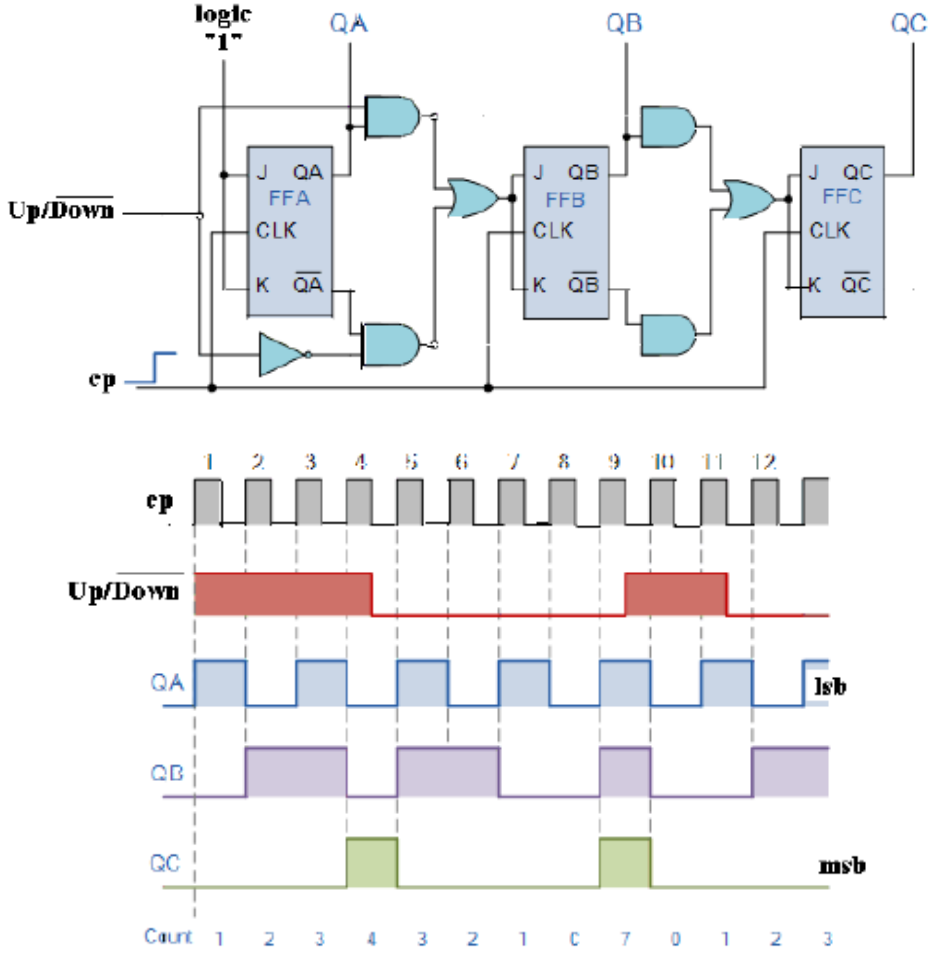

Figure 3:- 3-bit Synchronous Up/Down Counter and Output of Each Flip Flop

FF2	FF1	FF0
0	0	0
0	0	1
0	1	0
0	1	1
1	0	0
1	0	1
1	1	0
1	1	1

Figure 4:- Count Sequence

RESULTS:- Thus the 3-bit synchronous up/down counter is designed and verified.

PRECAUTIONS:-

1. All the connections should be made properly.
2. IC should not be reversed.

DEPARTMENT OF ELECTRICAL ENGINEERING

IIT (ISM), DHANBAD-826004

SEM: 3rd (B. TECH)

COURSE NAME: ANALOG AND DIGITAL ELECTRONICS LAB

COURSE CODE: EEC272
LOCATION: ROOM No. 115

EXPT. NO. 12

TITLE: To study 8-bit digital to analog converter

Apparatus required:

Sl. No.	Name of instruments	Quantity	Maker's Name	Sl. No.	Specification
1	Power supply				
2	Digital to analog converter(DAC0808)				
3	Multi-meter				
4	Breadboard				

Theory:

The electronic circuit that translates a digital signal to analog signal is called a Digital to Analog converter (DAC). One resistive technique for digital to analog conversion is weighted resistor DAC. DAC's in which the analog signal is allowed to vary is called multiplying DAC. In order to convert an 8-bit digital value to its respective analog value, DAC0808 chip is used. This device utilizes an R-2R ladder network to drive a current summing junction resulting in an appropriate analog value. Note that the DAC0808 D/A converter generate a varying analog current at its output, I_o, on Pin-4. The full-scale value of this current is determined by the current input at V_{ref+}, on Pin 14. Consequently, this current must be converted back to a voltage to obtain V_{out}. To do this, an LM741 operational amplifier is configured as a current to voltage converter using the same size current loop. The analog output corresponding to digital input is given by equation 1.

$$V_{out} = \left(\frac{D_7}{2} + \frac{D_6}{2^2} + \frac{D_5}{2^3} + \frac{D_4}{2^4} + \frac{D_3}{2^5} + \frac{D_2}{2^6} + \frac{D_1}{2^7} + \frac{D_0}{2^8} \right) \times V_{ref} \qquad (1)$$

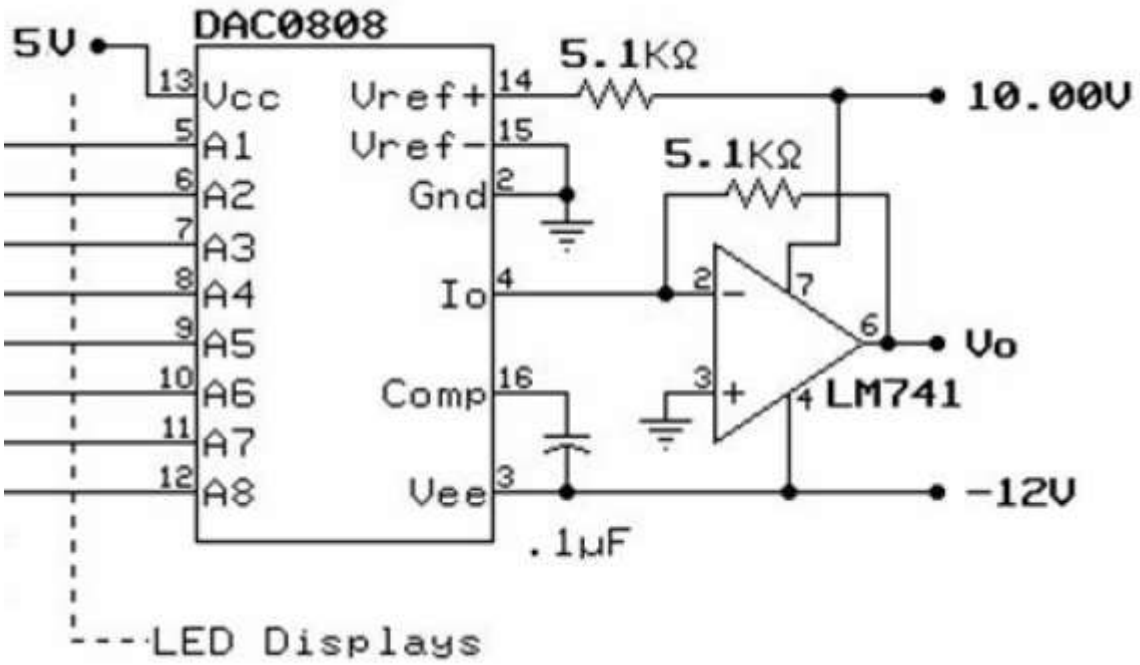

Figure 1: Digital to analog converter

PROCRDURE:

1. Connect the circuit as shown in the figure 1.
2. Set the digital input voltages using DC power supply.
3. Measure the output voltage corresponding to a digital input.
4. Calculate the output voltage corresponding to the digital input using equation 1.

OBSERVATION:

D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7	Analog output(V)

RESULT:

Thus, the study of digital to analog converter has been successfully performed and analog voltage to given input signal is obtained.